MODULE I

OPERATIONAL AMPLIFIERS (OP AMPS)

1.1 INTRODUCTION

The operational amplifier, most commonly referred as 'op-amp' was introduced in 1940s. The first operational amplifier was designed in 1948 using vacuum tubes. In those days, it was used in the analog computers to perform a variety of mathematical operations such as addition, subtraction, multiplication etc. Due to its use in performing mathematical operations it has been given a name operational amplifier. Due to the use of vacuum tubes, the early op-amps were bulky, power consuming and expensive.

Robert J. Widlar at Fairchild brought out the popular 741 integrated circuit (IC) op-amp between 1964 to 1968. The IC version of op-amp uses BJTs and FETs which are fabricated along with the other supporting components, on a single semiconductor chip or ¢ wafer which is of a pinhead size. With the help of IC op-amp, the circuit design becomes very simple. The variety of useful circuits can be built without the necessity of knowing about the complex internal circuitry. Moreover, IC op-amps are inexpensive, take up less space and consume less power. The IC op-amp has become an integral part of almost every electronic circuit which uses linear integrated circuit. The modern linear IC op-amp works at lower voltages. It is so low in cost that millions are now in use, annually.

Because of their low cost, small size, versatility, flexibility, and dependability, op-amps are used in the fields of process control, communications, computers, power and signal sources, displays and measuring systems.

1.2 OP-AMP SYMBOL AND TERMINALS

The symbol for an op-amp along with its various terminals, is shown in the Fig, 1.1. The op-amp is indicated basically by a triangle which points in the direction of the signal flow.

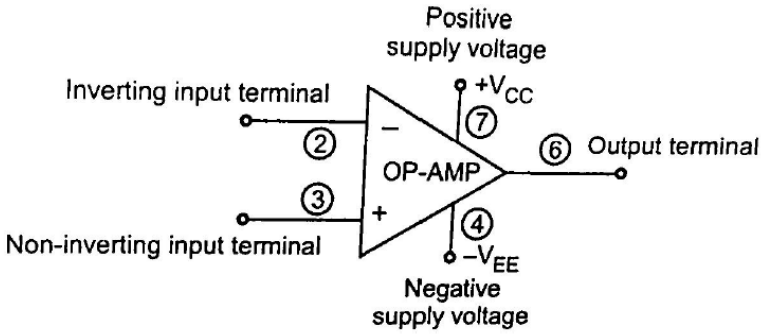


Fig: 1.1 Op-Amp Symbol

All the op-amps have at least following five terminals

- The positive supply voltage terminal Vcc or + V.
- The negative supply voltage terminal - V_{EE} or - V.

- The output terminal.
- The inverting input terminal, marked as negative.
- The noninverting input terminal, marked as positive.

The input at inverting input terminal results in opposite polarity (antiphase) output. While the input at noninverting input terminal results in the same polarity (phase) output. This is shown in the Fig. 1.2 (a) and (b). The input and output are in antiphase means having 180° phase difference in between them while in-phase input and output means having 0° phase difference in between them.

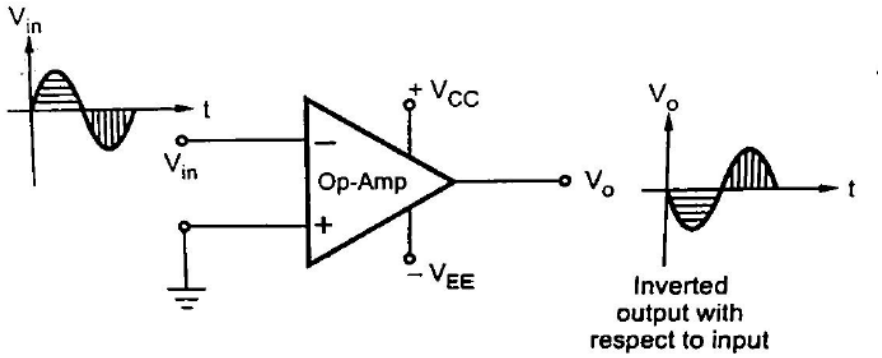


Fig 1.2(a): Input applied to Inverting Terminal

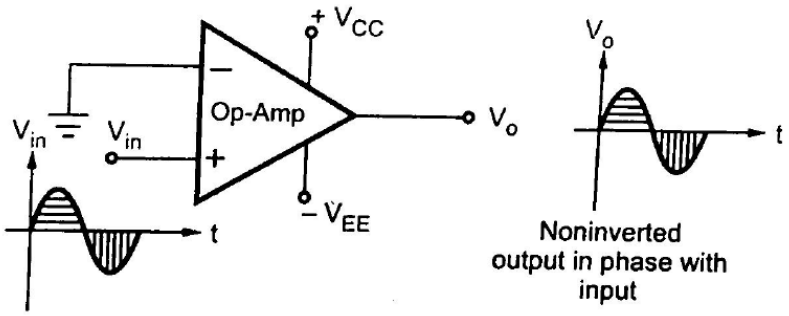


Fig 1.2(b): Input applied to Inverting Terminal

1.3 BLOCK DIAGRAM REPRESENTATION OF OP-AMP

As mentioned earlier, now a days op-amps are available in an integrated circuit form. Commercial integrated circuit op-amps usually consists of four cascaded blocks. The block diagram of IC op-amp is shown in the Fig. 1.3

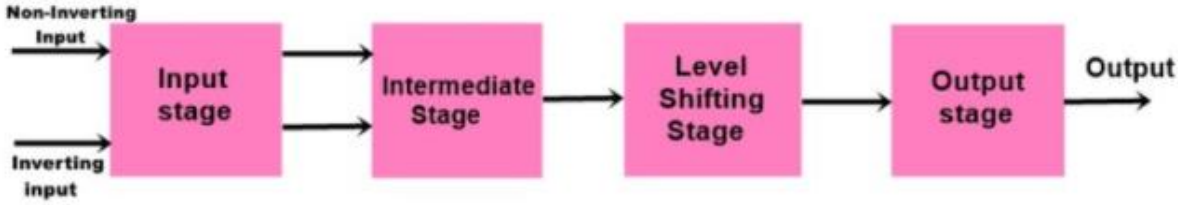


Fig 1.3: Internal Block diagram schematic of Op-Amp

1.3.1 Input Stage

The input stage requires high input impedance to avoid loading on the sources. It requires two input terminals. It also requires low output impedance. All such requirements are achieved by using the dual input, balanced output differential amplifier as the input stage. The function of a differential amplifier is to amplify the difference between the two input signals. The differential amplifier has high input impedance. This stage provides most of the voltage gain of the amplifier.

1.3.2 Intermediate Stage

The output of the input stage drives the next stage which is an intermediate stage. This is another differential amplifier with dual input, unbalanced i.e. single ended output. The overall gain requirement of the op-amp is very high. The input stage alone cannot provide such a high gain. The main function of the intermediate stage is to provide an additional voltage gain required. Practically, the intermediate stage is not a single amplifier but the chain of cascaded amplifiers called multistage amplifiers.

1.3.3 Level Shifting Stage

All the stages are directly coupled to each other. As the op-amp amplifies d.c. signals also, the coupling capacitors are not used to cascade the stages. Hence the d.c. quiescent voltage level of previous stage gets applied as the input to the next stage. Hence stage by stage d.c. level increases well above ground potential. Such a high d.c. voltage level may drive the transistors into saturation. This further may cause distortion in the output due to clipping. This may limit the maximum a.c. output voltage swing without any distortion. Hence before the output stage, it is necessary to bring such a high d.c. voltage level to zero volts with respect to ground.

The level shifter stage brings the d.c. level down to ground potential, when no signal is applied at the input terminals. Then the signal is given to the last stage which is the output stage.

The buffer is usually an emitter follower whose input impedance is very high. This prevents loading of the high gain stage.

1.3.4 Output Stage

The basic requirements of an output stage are low output impedance, large a.c. output voltage swing and high current sourcing and sinking capability. The push-pull complementary amplifier meets all these requirements and hence used as an output stage. This stage increases the output voltage swing and keeps the voltage swing symmetrical with respect to ground. The stage raises the current supplying capability of the op-amp

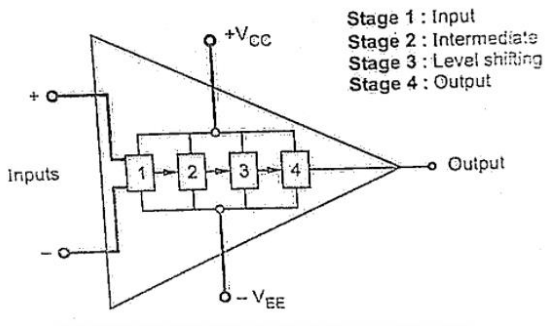


Fig 1.4: Overall Block diagram of an Op-amp

1.4 IDEAL OP-AMP

The ideal op-amp is basically an amplifier which amplifies the difference between the two input signals. In its basic form, the op-amp is nothing but a differential amplifier.

Ideal Op-amp Characteristics

An ideal op-amp has two input signals V_1 and V_2 applied to non-inverting and inverting terminals, respectively.

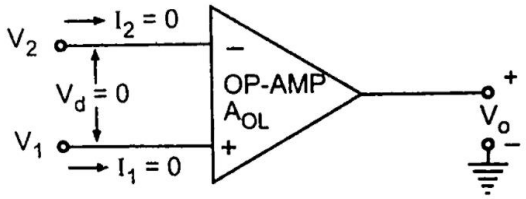


Fig 1.5: Ideal Op-amp

1. An ideal op-amp draws no current at both the input terminals i.e. $I_1 = I_2 = 0$. Thus its input impedance is infinite. Any source can drive it and there is no loading on the driver stage.
2. The gain of an ideal op-amp is infinite (∞), hence the differential input Vd =V_1 - V_2 is essentially zero for the finite output voltage Vo
3. The output voltage Vo is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits.

These properties are expressed generally as the characteristics of an ideal op-amp. The various characteristics of an ideal op-amp are:

a) Infinite voltage gain: It is denoted as A_{OL}. It is the differential open loop gain and is infinite for an ideal op-amp.

b) Infinite input impedance : The input impedance is denoted as Rin and is infinite for an ideal op-amp. This ensures that no current can flow into an ideal op-amp.

c) Zero output impedance : The output impedance is denoted as Ro and is zero for an ideal op-amp. This ensures that the output voltage of the op-amp remains same, irrespective of the value of the load resistance connected.

d) Zero offset voltage : The presence of the small output voltage though V1 = V2= 0 is called an offset voltage. It is zero for an ideal op-amp. This ensures zero output for zero input signal voltage.

e) Infinite Bandwidth

The range of frequency over which the amplifier performance is satisfactory is called its bandwidth. The bandwidth of an ideal op-amp is infinite. This means the operating frequency range is from 0 to ∞ . This ensures that the gain of the op-amp will be constant over the frequency range from d.c. (zero frequency) to infinite frequency. So op-amp can amplify d.c. as well as a.c. signals.

f) Infinite CMRR : The ratio of differential gain and common mode gain is defined as CMRR. Thus infinite CMRR of an ideal op-amp ensures zero common mode gain. Due to this common mode noise output voltage is zero for an ideal op-amp.

g) Infinite slew rate: This ensures that the changes in the output voltage occur, simultaneously with the changes in the input voltage. The slew rate is important parameter of op-amp. When the input voltage applied is step type which changes instantaneously then the output also must change rapidly as input changes. If output does not change with the same rate as input then there occurs distortion in the output. Such a distortion is not desirable. ***Infinite slew rate indicates that output changes simultaneously with the changes in the input voltage.***

The parameter slew rate is actually defined as the maximum rate of change of output voltage with time and expressed in V/μs.

$$Slew\ Rate = S = \left.\frac{dV_0}{dt}\right|_{maximum}$$

Slew Rate Equation

Let Vs be the input Voltage & Vo be the output voltage

$$Vs = Vm\ Sin\ \omega t$$

$$Vo = Vm\ Sin\ \omega t(\text{ output of Voltage follower})$$

$$\frac{dVo}{dt} = Vm(\omega cos\omega t)$$

But $\left.\frac{dVo}{dt}\right|_{Max} = Slew\ Rate$, for maximum value of $\frac{dVo}{dt}$, $cos\omega t = 1$;

Therefore $S = \left.\frac{dVo}{dt}\right|_{Max} = \omega Vm$

$$S = 2\pi f V_m \times 10^{-6} \quad V/\mu S$$

h) Power Supply Rejection Ratio (PSRR) :

The power supply rejection ratio is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called Power Supply Sensitivity.

So if VEE is constant and due to change in Vcc, there is change in input offset voltage then PSRR is expressed as,

$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{CC}}\Big|_{V_{EE}\ constant}$$

if Vcc is constant and due to change in VEE, there is change in input offset voltage then PSRR is expressed as

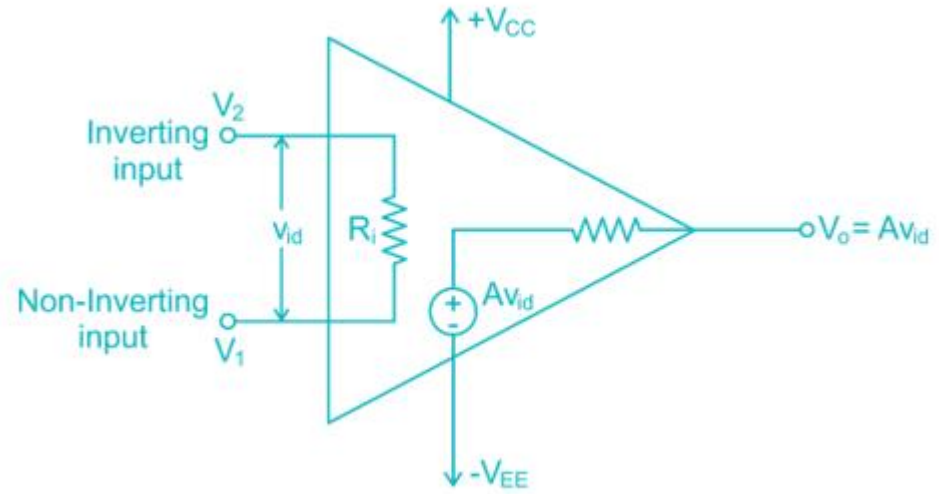
$$PSRR = \frac{\Delta V_{ios}}{\Delta V_{EE}}\Big|_{V_{CC}\ constant}$$

It is expressed in mV/V or μV/V and its ideal value is zero.

Ideal & Practical Characteristics can be summarized as

Characteristics	Symbol	Ideal Parameter Values	741 Parameter Values
Open loop voltage gain	AOL	∞	200000
Input Impedance	Rin	∞	2MΩ
Output Impedance	Ro	0	75Ω
Offset Voltage	Voo	0	2mV-6mV
Bandwidth	B.W	∞	1MHz
CMRR	ρ	∞	90dB
Slew Rate	S	∞	0.5V/μS
Power Supply Rejection Ratio	PSRR	0	150μV/V

1.5 EQUIVALENT CIRCUIT OF OPAMP



- Op-Amp Can be Modelled as Voltage controlled Voltage source (VCVS)
- $AV_{id} - Equivalent\ Thevenian\ Voltage\ source$

- Ro- output Resistance
- Vo= AV_{id}=$A(V_1-V_2)$
- Vid= Difference Voltage between inverting & non inverting Terminals

1.6 OPEN LOOP CONFIGURATIONS

The term open loop indicates 'no connection', either direct or via another network that exists between the output and input terminals. That is, the output signal is not a feedback in any form as part of the input signal.

When connected in open loop configuration, the op-amp simply functions as a high gain amplifier. There are three open loop op-amp configurations:

- Differential amplifier
- Inverting amplifier
- Non-inverting amplifier

1.6.1 Differential amplifier

Fig. shows the open loop differential amplifier in which input signals V_{in1} and V_{in2} are applied to the positive and negative input terminals. Since the op-amp amplifies the difference between the two input signals, this configuration is called the differential amplifier

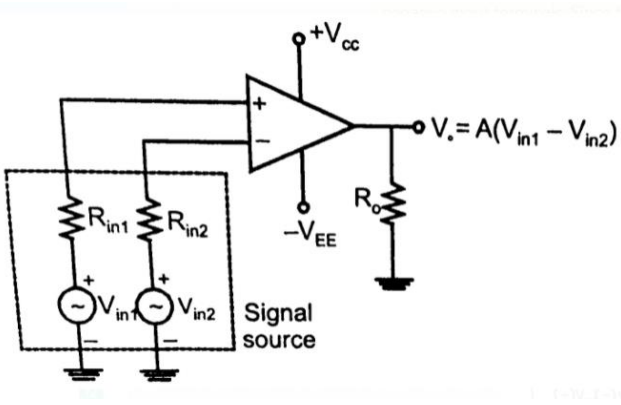


Fig 1.6 : Differential Amplifier using OP-Amp

The op-amp is a versatile device because it amplifies both ac and dc input signals. This means that V_{in1} and V_{in2} could be either ac or dc voltage. The source resistance R_{in1} and R_{in2} are normally negligible compared to the input resistance Ri. Therefore the voltage drop across these resistors can be assumed to be zero, which then implies that $V_1 = V_{in1}$ and $V_2 = V_{in2}$. Substituting these value in equation

$$V_0 = AV_{id} = A(V_1 - V_2)$$

$$V_0 = AV_{id} = A(V_{in1} - V_{in2})$$

1.6.2 Inverting Amplifier

In the inverting amplifier, input voltage is applied in the inverting input terminal. The non- inverting terminal is grounded. Since $V_1 = 0$ and $V_2 = Vin$

$$V_0 = AV_{id} = A(V_1 - V_2)$$

$$V_0 = AV_{id} = -AV_2$$

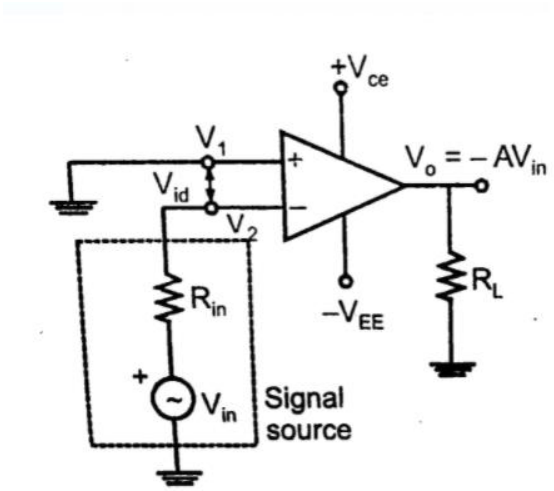


Fig 1.7: Inverting Amplifier

The negative sign indicates that the output voltage is out of phase with respect to input by 180° or is of opposite polarity. Thus in the inverting amplifier the input signal is amplified by gain A and is also inverted at the output

1.6.3 Non inverting amplifier

Fig shows the open loop non-inverting amplifier. In this configuration the input signal is to the non-inverting (positive) input terminal, and the inverting terminal is connected to ground

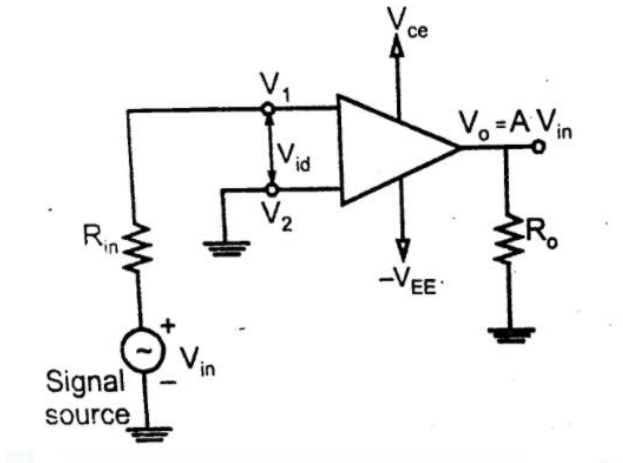


Fig 1.8: Non-Inverting Amplifier

From the circuit $V_1 = V_{in}$ *and* $V_2 = 0$

$$V_0 = A(V_1 - V_2) = AV_1$$

This means that the output voltage is larger than the input voltage by gain A and is in phase with the input signal.

1.7 VOLTAGE TRANSFER CURVE

The ideal op-amp produces the output proportional to the difference between the two input voltages. The graphical representation of this statement gives the voltage transfer curve. It is the graph of output voltage Vo plotted against the difference input voltage Vd, assuming gain constant. This graph is called transfer characteristics of the op-amp.

Now the output voltage is proportional to difference input voltage but only upto the positive and negative saturation voltages of op-amp. These saturation voltages are specified by the manufacturer Vo in terms of output voltage swing rating of an op-amp, for given value of supply voltages .These saturation voltages are slightly less than the supply voltages.

Thus, the voltage transfer curve is a straight line till output reaches saturation voltage level. Thereafter output remains ideal voltage transfer curve is shown in the Fig 1.9

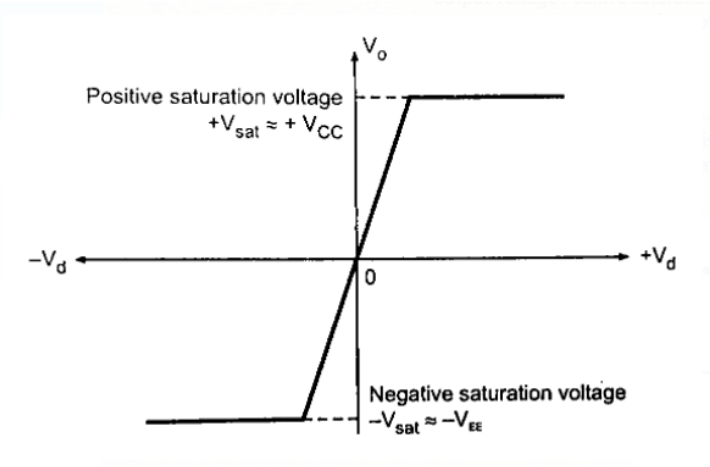


Fig 1.9: Ideal Voltage Transfer Curve

1.8 FREQUENCY RESPONSE CURVE

Ideally, an op-amp should have an infinite bandwidth. This means the gain of op-amp must remain same for all the frequencies from zero to infinite. Till now we have assumed gain of the op-amp as constant but practically op-amp gain decreases at higher frequencies. Such a gain reduction with respect to frequency is called roll off.

This happens because gain of the op-amp depends on the frequency and hence mathematically it is a complex number. Its magnitude and phase changes with frequency.

The plot showing the variations in magnitude and phase angle of the gain due to the change in frequency is called frequency response of the op-amp.

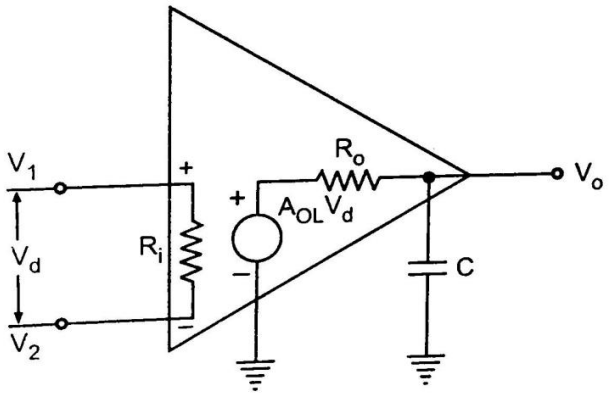


Fig 1.10: High Frequency model of Op-Amp

To obtain the frequency response, consider the high frequency model of the op-amp with a capacitor C at the output, taking into account the capacitive effect present. It is shown in the Fig.1.10 .

Let -jXc be the capacitive reactance due to the capacitor C. From the Fig. 1.10, using voltage divider rule

$$V_0 = A_{OL}V_d \frac{-jX_C}{R_0 - jX_C} \quad ; X_C = 2\pi fC$$

$$V_0 = A_{OL}V_d \times \frac{\frac{1}{j2\pi fC}}{R_0 + \frac{1}{j2\pi fC}} = \frac{A_{OL}V_d}{1 + j2\pi fR_0C}$$

$$A_{OL}(f) = \frac{V_0}{V_d} = \frac{A_{OL}}{1 + j2\pi fR_0C}$$

Let $f_C = \frac{1}{2\pi R_0 C}$= Cut off frequency of Op amp

$$A_{OL}(f) = \frac{V_0}{V_d} = \frac{A_{OL}}{1 + j\frac{f}{f_C}}$$

$$|A_{OL}(f)| = \frac{A_{OL}}{\sqrt{1 + \left(\frac{f}{f_C}\right)^2}}$$

As the frequency increases till f_C the gain is almost constant but after f_C the gain reduces with a rate of -20 dB/decade

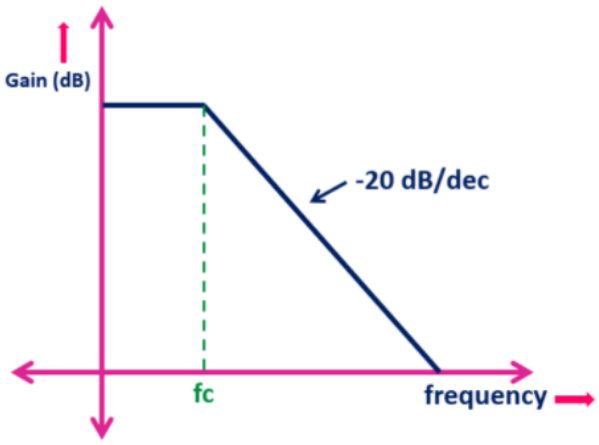


Fig 1.11 Frequency Response of Op-Amp

1.9 DIFFERENTIAL AMPLIFIERS

The Differential Amplifier Amplifies the difference between two input voltage signals. Hence It is called Differential Amplifier.

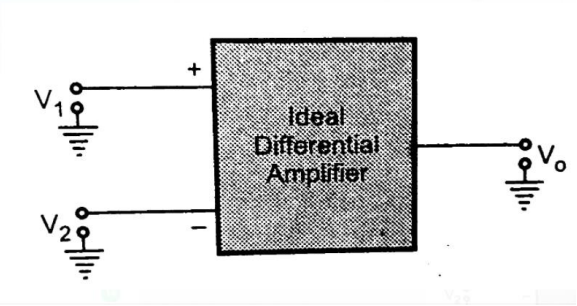


Fig :1.12 Ideal Differential Amplifier

V_1 and V_2 are the two input signals while V_0, is the single ended output. Each signal is measured with respect to the ground. In an ideal differential amplifier, the output voltage V_0, is proportional to the difference between the two input Signals. Hence we can write,

$V_0 = A_d(V_1 - V_2)$-------(1)

$V_0 \propto (V_1 - V_2)$

Differential Gain (Ad)

From Equation 1 we can write $V_0 = A_d(V_1 - V_2)$ where Ad is the gain which differential amplifier amplifies the difference between the two input signals. Hence called Differential Gain

$$V_0 = A_d V_d$$

$$A_d = \frac{V_0}{V_d}$$

Generally Differential Gain is expressed in dB.

$$A_d = 20\log(Ad) \qquad in\ dB$$

Common Mode Gain Ac.

If we apply two input voltages which are equal in all the respects to the differential amplifier i.e. $V_1 = V_2$, then ideally the output voltage $V_0 = (V_1 - V_2)$ Aa must be zero. But the output voltage of the practical differential amplifier not only depends on the difference voltage but also depends on the average common level of the two inputs. Such an average level of the two input signals is called common mode signal denoted as Vc

$$V_C = \frac{V_1 + V_2}{2}$$

The gain with which it amplifies the common mode signal to produce the output is called common mode gain of the differential amplifier denoted as Ac

$$Vo = AcVc$$

$$Ac = \frac{Vo}{Vc}$$

So the Total output of any differential amplifier can be expressed as

$$Vo = AdVd + AcVc$$

Common Mode Rejection Ratio CMRR

When the same voltage is applied to both the inputs, the differential amplifier is said to be operated in a common mode configuration. Many disturbance signals, noise signals _ appear as a common input signal to both the input terminals of the differential amplifier. Such a common signal should be rejected by the differential amplifier

The ability of a differential amplifier to reject a common mode signal is expressed by a ratio called common mode rejection ratio denoted as CMRR. It is defined as the ratio of the differential voltage gain Ad to common mode voltage gain Ac.

$$CMRR = \rho = \left|\frac{Ad}{Ac}\right|$$

Ideally the common mode voltage gain is zero, hence the ideal value of CMRR is infinite. For a practical differential amplifier Ad is large and Ac is small hence the value of CMRR is also very large. Many a times, CMRR is also expressed in dB

$$CMRR\ in\ dB = 20\ log\left|\frac{Ad}{Ac}\right|\ dB$$

The output Voltage can be expressed in terms of CMRR

$$Vo = Advd + AcVc = AdVd\left\{1 + \frac{AcVc}{AdVd}\right\}$$

$$Vo = AdVd\left\{1 + \frac{1}{\left(\frac{Ad}{Ac}\right)} \times \frac{Vc}{Vd}\right\}$$

$$Vo = AdVd\left[1 + \frac{1}{CMRR} \times \frac{Vc}{Vd}\right]$$

Features of Differential Amplifier

The various features of a differential amplifier are

- High differential voltage gain.
- Low common mode gain.
- High CMRR
- Two input terminals.
- High input impedance.
- Large bandwidth.
- Low offset voltages and currents.
- Low output impedance.

1.9.1 TRANSISTORISED DIFFERENTIAL AMPLIFIER

The transistorised differential amplifier basically uses the emitter biased circuits which are identical in characteristics. Such two identical emitter biased circuits are shown in the Fig

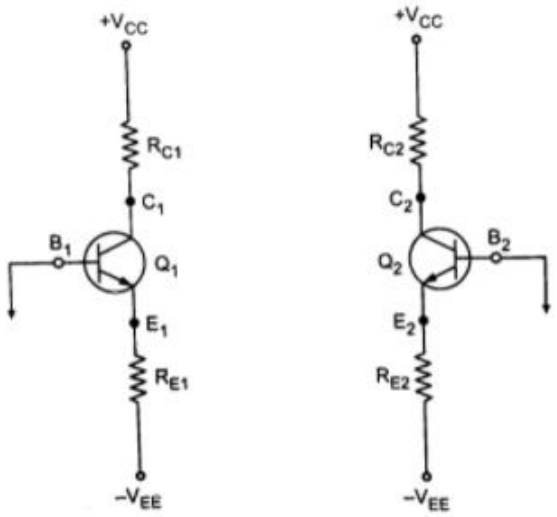


Fig 1.13: Emitter Based Circuits

The two transistors Q_1 and Q_2 have exactly matched characteristics. The two collector resistances R_{c1} and R_{c2} are equal while the two emitter resistances R_{E1} and R_{E2} are also equal.

Thus R_{C1}, = R_{C2} and R_{E1}= R_{E2}

The magnitudes of + Vcc and - V_{EE} are also same. The differential amplifier can be obtained by using such two emitter biased circuits. This is achieved by connecting emitter E_1 of Q_1 to the emitter E_2 of Q_2. Due to this, R_{E1} appears in parallel with R_{E2}, and the combination can be replaced by a single resistance denoted as R_E. The base B_1 of Q_1 is connected to the input 1 which is V_{S1}, while the base B_2 of Q_2 is connected to the input 2 which is V_{s2}. The supply voltages are measured with respect to ground. The balanced output is taken between the collector C_1 of Q_1 and the collector C_2, of Q_2. Such an amplifier is called emitter coupled differential amplifier. The two collector resistances are same hence can be denoted as Rc.

The output can be taken between two collectors or in between one of the two collectors and the ground. When the output is taken between the two collectors, none of them is grounded then it is called balanced output, double ended output or floating output.

When the output is taken between any of the collectors and the ground, it is called unbalanced output or single ended output. The complete circuit diagram of such a basic dual input, balanced output differential amplifier is shown in the Fig.

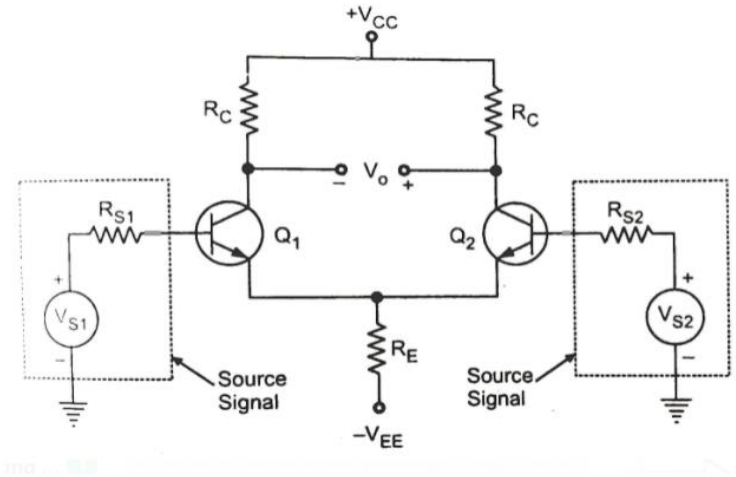


Fig 1.14: Dual input Balanced output Differential Amplifier

As the output is taken between two output terminals, none of them is grounded, it is called balanced output differential amplifier.

Let us study the circuit operation in the two modes namely

- Differential mode operation
- Common mode operation

Differential Mode Operation

In the differential mode, the two input signals are different from each other. Consider the two input signals which are same in magnitude but 180° out of phase. These signals, with opposite phase can be obtained from the center tap transformer. The circuit used in differential mode operation is shown in the Fig.

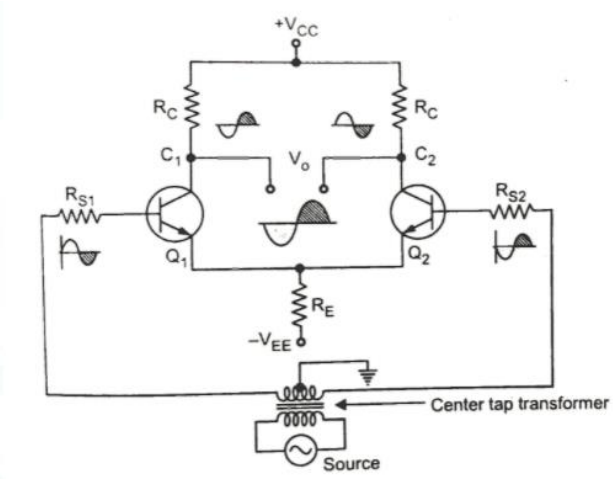


Fig 1.15: Differential Mode Operation

Assume that the sine wave on the base of Q1 is positive going while on the base of Q2 is negative going. With a positive going signal on the base of Q1, an amplified negative going signal develops on the collector of Q1. Due to positive going signal, current through R_E, also increases and hence a positive going wave is developed across R_E. Due to negative going signal on the base of Q2, an amplified positive going signal develops on the collector of Q2. And a negative going signal develops across RE, because of emitter follower action of Q2.

So signal voltages across RE, due to the effect of Q1 and Q2 are equal in magnitude and 180° out of phase, due to matched pair of transistors. Hence these two signals cancel each other and there is no signal across the emitter resistance. Hence there is no a.c. signal current flowing through the emitter resistance. Hence RE in this case does not introduce negative feedback.

While Vo is the output taken across collector of Q1 and collector of Q2. The two outputs on collector 1 and 2 are equal in magnitude but opposite in polarity. And Vo is the difference between these two signals, e.g. +10 - (-10) = + 20. Hence the difference output Vo is twice as large as the signal voltage from either collector to ground.

Common Mode Operation

In this mode, the signals applied to the base of Q1and Q2 are derived from the same source. So the two signals are equal in magnitude as well as in phase. The circuit diagram is shown in fig.

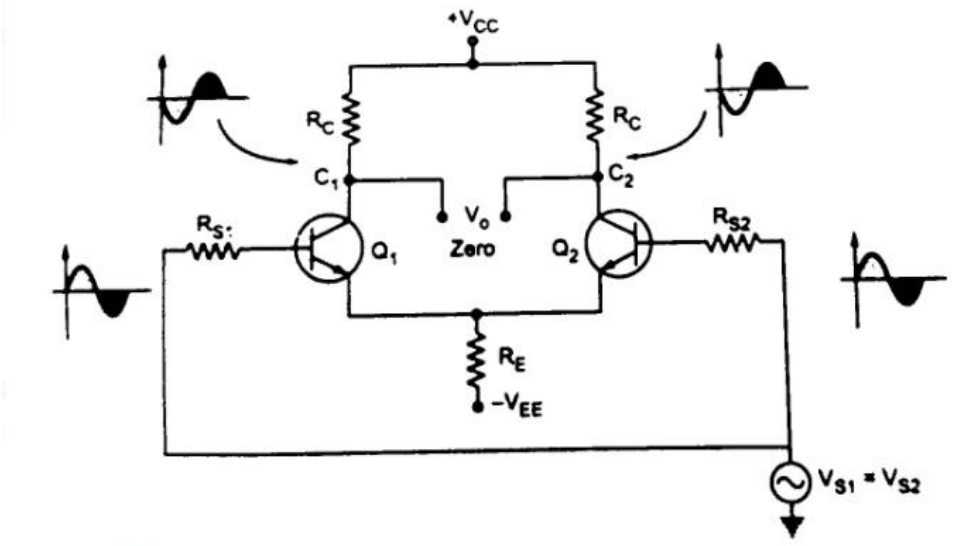


Fig 1.16: Common ode Operation

In phase signal voltages at the bases of Q1 and Q2 causes in phase signal voltages to appear across RE, which add together. Hence RE carries a signal current and provides a negative feedback. This feedback reduces the common mode gain of differential amplifier. While the two signals causes in phase signal voltages of equal magnitude to appear across the two collectors of Q1 and Q2. Now the output voltage is the difference between the two collector voltages, which are equal and also same in phase, e.g. (10) -(10) = 0. Thus the difference output Vo is almost zero, negligibly small. ***Ideally it should be zero.***

Types of Differential Amplifiers

The differential amplifier, in the difference amplifier stage in the op-amp, can be used in four configurations.

- Dual input, balanced output differential amplifier.
- Dual input, unbalanced output differential amplifier
- Single input, balanced output differential amplifier.
- Single input, unbalanced output differential amplifier.

The differential amplifier uses two transistors in common emitter configuration. If output is taken between the two collectors it is called balanced output or double ended output. While if the output is taken between one collector with respect to ground it is called unbalanced output or single ended output. If the signal is given to both the input

terminals it is called dual input, while if the signal is given to only one input terminal and other terminal is grounded it is called single input or single ended input.

Out of these four configurations the dual input, balanced output is the basic differential amplifier configuration. This is shown in the Fig. 1.17 (a). The dual input, unbalanced output differentia: amplifier is shown in the Fig. 1.17 (b). The single input, balanced output differential amplifier is shown in the Fig. 1.17 (c) and the single input, unbalanced output differential amplifier is shown in the Fig. 1.17 (d).

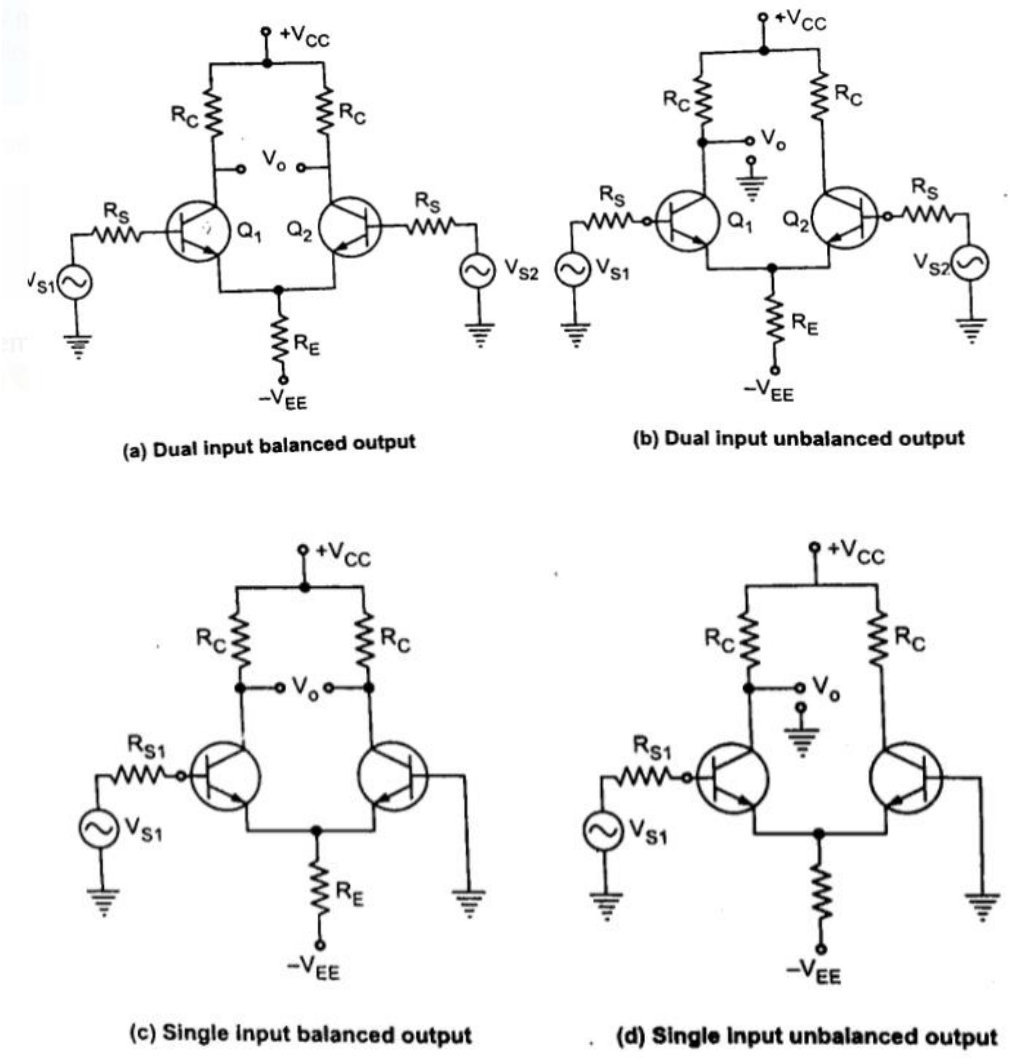


Fig 1.17

The operation of dual input balanced output differential amplifier in differential mode and common mode is already discussed in the last section. This configuration is also called symmetrical differential amplifier.

1.10 D.C. ANALYSIS OF DIFFERENTIAL AMPLIFIER

The d.c. analysis means to obtain the operating point values i.e. I_{CQ} and V_{CEQ} for the transistors used. The supply voltages are d.c. while the input signals are a.c., so d.c. equivalent circuit can be obtained simply by reducing the input a.c. signals to zero. The

d.c. equivalent circuit thus obtained is shown in the Fig. 1.18. Assuming R_{S1}, = R_{S2}, the source resistance is simply denoted by Rs.

The transistors Q_1 and Q_2 are matched transistors and hence for such a matched pair we can assume

- Both the transistors have the same characteristics.
- $R_{E1} = R_{E2}$ hence $R_E = R_{E1} \,||\, R_{E2}$.
- $R_{C1} = R_{C2}$ hence denoted as R_C.
- $|V_{CC}| = |V_{EE}|$ and both are measured with respect to ground.

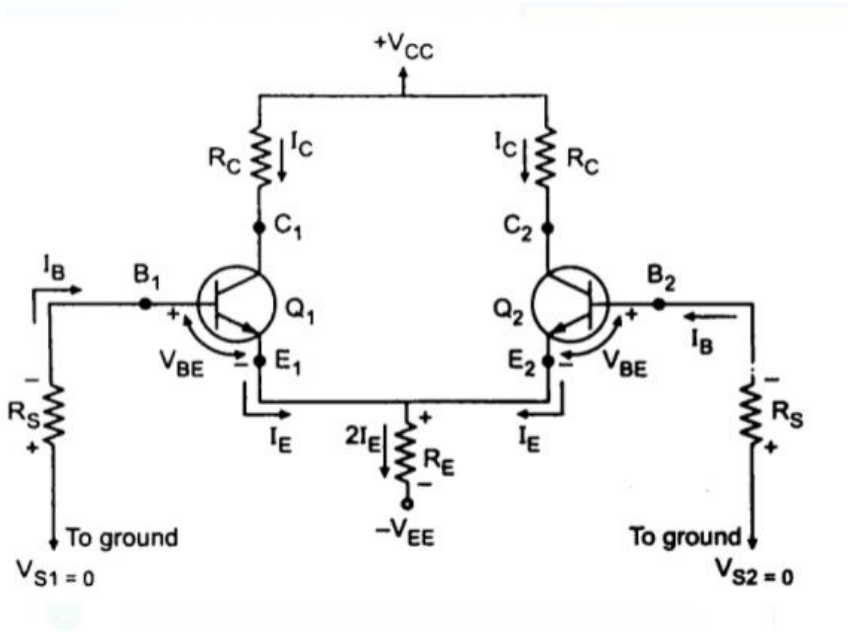


Fig 1.18: DC equivalent Circuit

As the two transistors are matched and circuit is symmetrical, it is enough to find out operating point I_{CQ} and V_{CEQ}, for any one of the two transistors. The same is applicable for the other transistor. Applying KVL to base-emitter loop of the transistor Q_1

$$-I_B R_S - V_{BE} - 2I_E R_E + V_{EE} = 0 \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

But $I_C = \beta I_B \cong I_C \quad ; \; I_B = \frac{I_E}{\beta}$

Therefore Equation (1) becomes

$$\frac{-I_E R_S}{\beta} - V_{EE} - 2I_E R_E + V_{EE} = 0 \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

$$I_E \left[\frac{-R_S}{\beta} - 2R_E\right] + V_{EE} - V_{BE} = 0 \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

$$I_E = \frac{V_{EE} - V_{BE}}{\frac{R_S}{\beta} + 2R_E} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

Generally $\frac{R_S}{\beta} \ll 2R_E$

$\therefore I_E = \frac{V_{EE}-V_{BE}}{2R_E}$.....(5)

From the equation (5), we can observe that

i) R_E determines the emitter current of Q_1 and Q_2 for the known value of V_{EE}.
ii) The emitter current through Q1 and Q2 is independent of collector resistance R_C.

Now let us determine V_{CE}. As I_E is known and $I_E = I_C$, we can determine the collector voltage of Q_1

$$V_C = V_{CC} - I_C R_C \ldots\ldots (6)$$

Neglecting the drop across Rs, we can say that the voltage at the emitter of Q1 is approximately equal: to $-V_{BB}$. Hence the collector to emitter voltage is

$$\therefore V_{CE} = V_C - V_E = (V_{CC} - I_C R_C) - (-V_{BE})$$

$$\therefore V_{CE} = V_{CC} + V_{BE} - I_C R_C \ldots\ldots\ldots (7)$$

Hence $I_E = I_C = I_{CQ}$ *while* $V_{CE} = V_{CEQ}$ *for given values of* V_{CC} *and* V_{EE}

Key Point: In the equation (5), the sign of V_{EE} is already considered to be negative, while deriving it. Hence while using this equation to solve the problem, only the magnitude of V_{EE} should be used and negative sign of V_{EE} should not be used again.

Thus for both the transistors, we can determine operating point values, using equations (5) and (7). With the same biasing arrangement, the d.c. analysis remains same for all the four possible configurations of differential amplifier

$$I_E = \frac{V_{EE} - V_{BE}}{2R_E} \approx I_{CQ}$$

$$V_{CE} = V_{CC} + V_{BE} - I_{CQ} R_C$$

1.11 A.C. ANALYSIS OF DIFFERENTIAL AMPLIFIER USING H-PARAMETERS

In the a.c. analysis we will calculate the differential gain Ad, common mode gain Ac, input resistance Ri and the output resistance Ro of the differential amplifier circuit, using the h-parameters..

Differential Gain (Ad)

For the differential gain calculation, the two input signals must be different from each other. Let the two a.c. input signals be equal in magnitude but having 180° phase difference in between them. The magnitude of each a.c. input voltage V_{S1} and V_{S2} be Vs /2.

The two a.c. emitter currents $I_{e1}$and I_{e2} are equal in magnitude and 180° out of phase. Hence they cancel each other to get resultant a.c. current through the emitter as zero. Hence for the a.c. purposes emitter terminal can be grounded. The a.c. small signal differential amplifier circuit with grounded emitter terminal is shown in the Fig.1.19

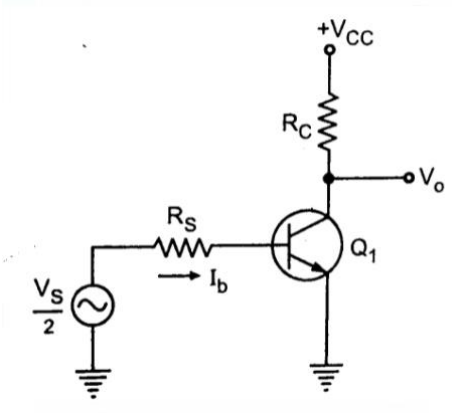


Fig 1.19: AC equivalent circuit for differential operation

As the two transistors are matched, the a.c. equivalent circuit for the other transistor is identical to the one shown in the Fig. 1.19. Thus the circuit can be analysed by considering only one transistor. This is called as half circuit concept of analysis.

The approximate hybrid model for the above circuit can be shown as in the Fig. 1.19, neglecting hoe,

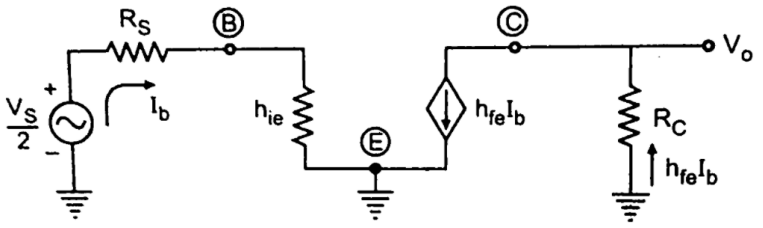


Fig 1.19: Approximate hybrid model

Applying KVL to the input Loop

$$-I_b R_S - I_b h_{ie} + \frac{V_S}{2} = 0 \ldots\ldots\ldots\ldots\ldots (1)$$

$$-I_b(R_S + h_{ie}) = -\frac{V_S}{2}$$

$$I_b = \frac{V_S}{2(R_S + h_{ie})} \ldots\ldots\ldots\ldots (2)$$

Applying KVL to output Loop

$$V_0 = -h_{fe} I_b R_C \ldots\ldots (3)$$

Sub eqn (2) in (3)

$$V_0 = -h_{fe} \frac{V_S}{2(R_S + h_{ie})} R_C$$

$$\frac{V_0}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \ldots\ldots\ldots (4)$$

The negative sign indicates the phase difference between input and output. Now two input signal magnitudes are $\frac{V_S}{2}$ but they are opposite in polarity, as 180° out of phase.

$$\therefore V_d = V_1 - V_2 = \frac{V_S}{2} - \left(-\frac{V_S}{2}\right) = V_S$$

The magnitude of the Differential gain Ad is

$$A_d = \frac{V_0}{V_S} = \frac{-h_{fe} R_C}{2(R_S + h_{ie})} \ldots\ldots\ldots (5)$$

What we are interested is to obtain Ad for the differential amplifier with the balanced output. Balanced output is across the two collectors of the transistors Q1 and Q2, which are perfectly matched. Such balanced output is double than that obtained above, with unbalanced output. Hence the-expression for Ad with balanced output changes as

$$A_d = 2 \times \frac{-h_{fe} R_C}{2(R_S + h_{ie})}$$

$$A_d = \frac{V_0}{V_S} = \frac{h_{fe} R_C}{(R_S + h_{ie})} \ (Magnitide) \ldots\ldots\ldots (6)$$

This is the Differential Gain for Dual input Balanced output Differential Amplifier Circuit.

Common Mode Gain (Ac)

Let the magnitude of both the a.c. input signals be Vs and are in phase with each other. Hence the differential input Va = 0 while the common mode input Vc is the average value of the two

$$\therefore V_C = \frac{V_1 + V_2}{2} = \frac{V_S + V_S}{2} = V_S \ldots\ldots (7)$$

While the output can be expressed as

$$V_0 = A_C V_S \ldots\ldots (8)$$

$$A_C = \frac{Vo}{Vs} \ldots (9)$$

But now both the emitter currents $I_{e1} = I_{e2} = Ie$, flows through R_E in the same direction. Hence the total current flowing through R_E is 2Ie.

As the two transistors are matched, ac. equivalent of common mode operation can be shown, considering only one transistor, as in the Fig. 1.20 operation can

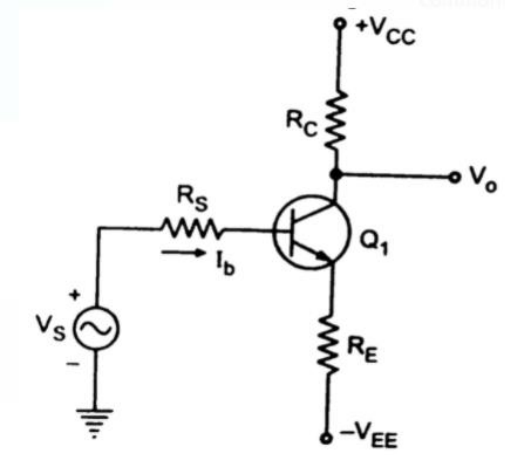


Fig 1.20: AC equivalent circuit for Common mode operation

The approximate hybrid model is

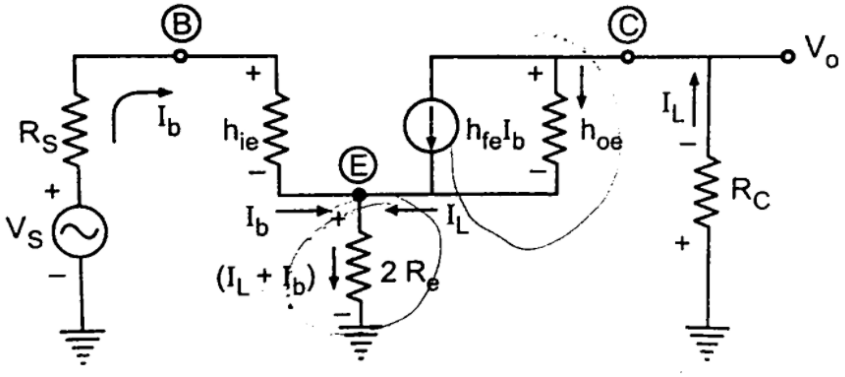


Fig 1.21: approximate hybrid model

As the current through R_E is 2Ie, for simplicity of derivation the current can be assumed to be Ie, and effective emitter resistance as 2 R_e. Hence the emitter resistance is shown 2 R_e in the Fig. 1.21.

So current through Re = load current I_L

effective emitter resistance = 2 Re

current through emitter resistance = I_L+I_b

$$\text{current through hoe} = (I_L - h_{fe}I_b)$$

Applying KVL to the input side,

$$-I_b R_S - I_b h_{ie} - 2R_e(I_L + I_b) + V_S = 0$$

$$V_S = I_b(R_S + h_{ie} + 2R_e) + I_L(2R_e) \ldots\ldots(10)$$

While $V_0 = -I_L R_C$.....(11)

Applying KVL in output loop

$$\frac{-(I_L - h_{fe} I_b)}{h_{oe}} - 2R_e(I_L + I_b) - I_L R_C = 0$$

$$\frac{-I_L}{h_{oe}} + \frac{h_{fe}}{h_{oe}} I_b - 2R_e I_L - 2R_e I_b - I_L R_C = 0$$

$$I_b\left[\frac{h_{fe}}{h_{oe}} - 2R_e\right] = I_L\left[\frac{1}{h_{oe}} + 2R_e + R_C\right]$$

$$I_b\left(h_{fe} - 2R_e h_{oe}\right) = I_L[1 + h_{oe}(2R_e + R_C]$$

$$\therefore \frac{I_L}{I_b} = \frac{\left(h_{fe} - 2R_e h_{oe}\right)}{[1 + h_{oe}(2R_e + R_C]}$$

$$I_b = \frac{I_L[1 + h_{oe}(2R_e + R_C]}{\left(h_{fe} - 2R_e h_{oe}\right)} \ldots\ldots\ldots(12)$$

Substitute the Value of Ib in equation (10)

$$V_S = \frac{I_L[1 + h_{oe}(2R_e + R_C]}{\left(h_{fe} - 2R_e h_{oe}\right)}(R_S + h_{ie} + 2R_e) + I_L(2R_e)$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}(2R_e + R_C]}{\left(h_{fe} - 2R_e h_{oe}\right)}(R_S + h_{ie} + 2R_e) + (2R_e)$$

$$\frac{V_S}{I_L} = \frac{[1 + h_{oe}2R_e + h_{oe}R_C] + (R_S + h_{ie} + 2R_e) + (2R_e)\left(h_{fe} - 2R_e h_{oe}\right)}{\left(h_{fe} - 2R_e h_{oe}\right)}$$

$$= \frac{R_s(1 + 2R_e h_{oe}) + R_s R_c h_{oe} + h_{ie}(1 + 2R_e h_{oe}) + h_{ie} h_{oe} R_C + 2R_e[1 + h_{oe}2R_e + h_{oe}R_C] + (2R_e)\left(h_{fe} - 2R_e h_{oe}\right)}{\left(h_{fe} - 2R_e h_{oe}\right)}$$

$$= \frac{R_s(1 + 2R_e h_{oe}) + R_s R_c h_{oe} + h_{ie}(1 + 2R_e h_{oe}) + h_{ie} h_{oe} R_C + 2R_e + 4{R_e}^2 h_{oe} + 2R_e h_{oe} R_C + 2R_e h_{fe} - 4{R_e}^2 h_{oe}}{\left(h_{fe} - 2R_e h_{oe}\right)}$$

$$= \frac{R_s(1+2R_eh_{oe}) + R_sR_ch_{oe} + h_{ie}(1+2R_eh_{oe}) + h_{ie}h_{oe}R_C + 2R_e + 2R_eh_{oe}R_C + 2R_eh_{fe}}{(h_{fe} - 2R_eh_{oe})}$$

$$= \frac{R_s(1+2R_eh_{oe}) + 2R_e(1+h_{fe}) + h_{ie}(1+2R_eh_{oe}) + h_{oe}R_C(2R_e + R_s + h_{ie})}{(h_{fe} - 2R_eh_{oe})}$$

$$= \frac{2R_e(1+h_{fe}) + (R_s + h_{ie})(1+2R_eh_{oe}) + h_{oe}R_C(2R_e + R_s + h_{ie})}{(h_{fe} - 2R_eh_{oe})}$$

Neglecting the terms of $h_{oe}R_C$ as practically $h_{oe}R_C \ll 1$

$$\frac{V_S}{I_L} = \frac{2R_e(1+h_{fe}) + (R_s + h_{ie})(1+2R_eh_{oe})}{(h_{fe} - 2R_eh_{oe})}$$

$$I_L = \frac{V_S(h_{fe} - 2R_eh_{oe})}{2R_e(1+h_{fe}) + (R_S + h_{ie})(1+2R_eh_{oe})}$$

Substituting the Value of I_L in Equation (11)

$$V_0 = \frac{-V_S(h_{fe} - 2R_eh_{oe})R_C}{2R_e(1+h_{fe}) + (R_S + h_{ie})(1+2R_eh_{oe})}$$

Hence the Common mode gain can be written by neglecting the terms of h_{oe}

$$A_c = \frac{V_0}{V_S} = \frac{-h_{fe}R_C}{2R_e(1+h_{fe}) + (R_S + h_{ie})} \ldots\ldots(13)$$

Common Mode Rejection Ratio(CMRR)

Once the Ad & Ac are obtained ,the expression for CMRR can be obtained as

$$CMRR = \left|\frac{A_d}{A_c}\right| \ldots\ldots(14)$$

$$CMRR = \frac{2R_e(1+h_{fe}) + (R_S + h_{ie})}{(R_S + h_{ie})} \ldots\ldots(15)$$

Differential Input Resistance (Ri)

It is the equivalent resistance between one of the input and the ground when the other input terminal is grounded.

$$R_i = \frac{V_S}{I_b} \ldots\ldots(16)$$

Sub eqn (2) in (16)

$$R_i = \frac{V_S}{\frac{V_S}{2(R_S + h_{ie})}}$$

$$R_i = 2(R_S + h_{ie}) \dots \dots .. (17)$$

Output Resistance (Ro)

It is defined as the equivalent resistance between one of the output terminals with respect to ground. As seen from the Fig. 1.19, the resistance between output terminal with respect to ground is Rc.

$$R_0 = R_C \dots \dots \dots (18)$$

1.12 METHODS OF IMPROVING CMRR

Higher the value of CMRR, better is the performance of differential amplifier. Hence in practice the efforts are always to improve the CMRR of the differential amplifier. Along with the basic circuit, various other circuits are used to improve the performance of differential amplifier.

EFFECT OF R_E

To improve the CMRR, the common mode gain Ac, must be reduced. The common mode gain Ac. approaches zero as R_E tends to infinity. This is because R_E introduces a negative feedback in the common mode operation which reduces the common mode gain Ac. Thus higher the value of R_E, lesser is the value of Ac, and higher is the value of CMRR. The differential gain Ad is not dependent on R_E. But practically R_E can not be selected very high due to certain limitations such as

1. Large Re needs higher biasing voltage to set the operating Q point of the transistors.

2. This increases the overall chip area.

Hence practically instead of increasing R_E various other methods are used which Provide effect of increased R_E without any limitations. Such two methods are

- Constant current bias method.
- Use of current mirror circuit.

Differential Amplifier with Constant Current Source

Without physically increasing the value of R_E, the R_E is replaced by a transistor Operated at a constant current. Such a constant current source circuit gives the effect of a very high resistance without affecting the Q point values of the differential amplifier. The

differential amplifier using constant current bias circuit instead of R_E is shown in figure 1.22.

The transistor used is Q3 and the values of R1, R2 and R3 are selected so as to give the same operating point values for the two transistors Q1 and Q2.

Circuit Analysis

Let current through R3 be I_{E3}; while current through R_1 is I. Neglecting the base current of Q3 which is very small due to large β_{ac}, we can assume that current through R_2 is also I.

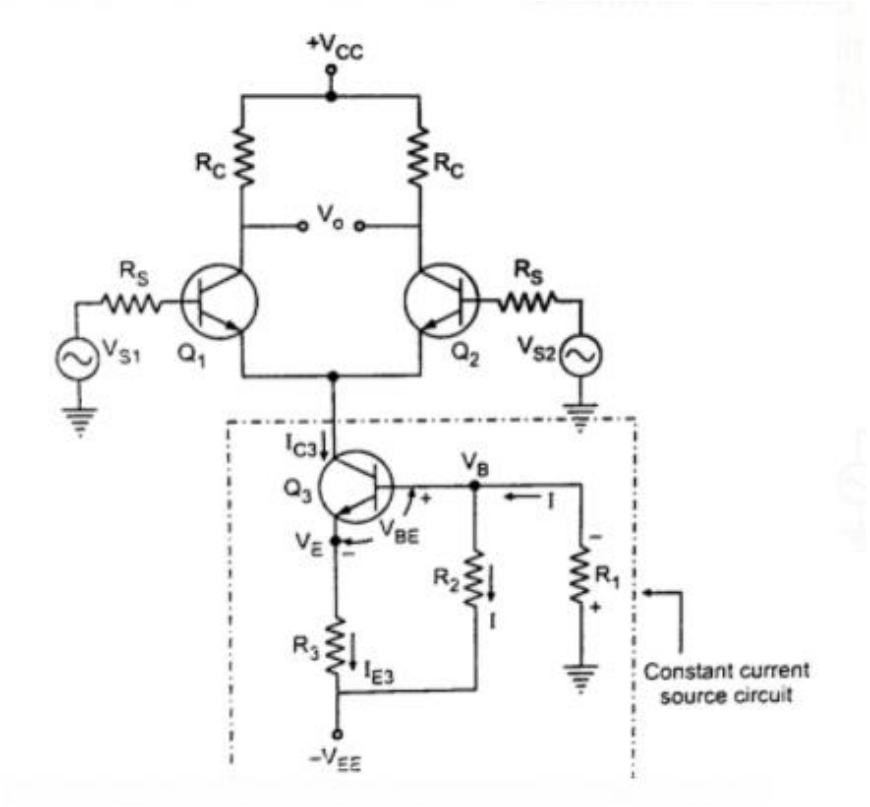


Fig 1.22 : Use of constant current source

Applying Kirchhoff's law

$$-IR_1 - IR_2 + V_{EE} = 0$$

$$I = \frac{V_{EE}}{R_1 + R_2}$$

Now $V_B = -IR_1$

$$V_B = -\frac{V_{EE}}{R_1 + R_2} R_1$$

Now $V_E = V_B - V_{BE}$

$$I_{E3} = \frac{V_E - (-V_{EE})}{R_3}$$

Substitute the values for V_B & V_E

$$I_{E3} = \frac{\frac{-V_{EE}}{R_1 + R_2} R_1 - V_{BE} + (V_{EE})}{R_3}$$

$$I_{E3} = \frac{V_{EE}\left[\frac{R_2}{R_1 + R_2}\right] - V_{BE}}{R_3}$$

Neglecting I_{B3} we can write

$$I_{C3} = I_{E3}$$

Thus as V_{EE}, R1, R2, R3 and V_{BE} are constants, current I_{C3} is almost equal to I_{E3}, and also constant. Thus circuit with transistor Q3, acts as a constant current source

Constant current Bias using Zener

The problem of temperature dependent characteristics of the transistor can be solved by using zener diode. This is because zeners are available over a wide range of voltages and can have a matching temperature coefficient of voltage to those of transistors. Constant current bias circuit using zener is shown

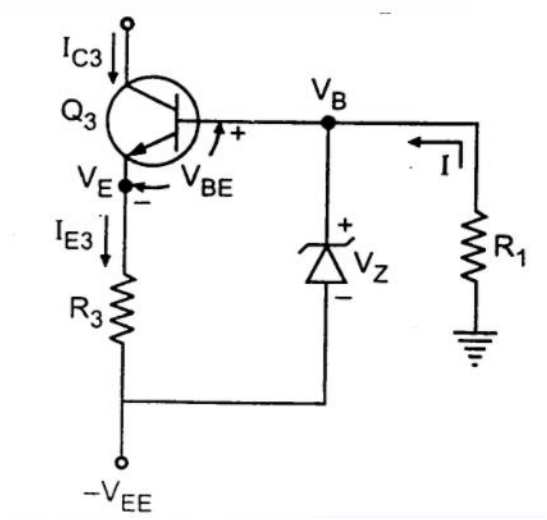


Fig 1.23: Constant current bias using Zener

Circuit Analysis

The Voltage at the base of transistor Q3

$$V_B = -V_{EE} + V_Z$$

$$V_E = V_B - V_{BE}$$

$$V_E = -V_{EE} + V_Z - V_{BE}$$

$$I_{E3} = \frac{V_E - (-V_{EE})}{R_3}$$

$$I_{E3} = \frac{-V_{EE} + V_Z - V_{BE} + V_{EE}}{R_3}$$

$$I_{E3} = \frac{V_Z - V_{BE}}{R_3}$$

While the value of R1 is selected in such a way that zener diode always conducts in reverse region,it can be calculated as

$$R_1 = \frac{V_{EE} - V_Z}{I}$$

The common mode gain is almost zero, providing very large value of CMRR, with a constant current bias. To offer extremely large resistance under a.c. conditions, a simple circuit of constant current source, with less number of components is now a days used. This circuit is called ***current mirror*** or ***current repeater circuit***

CURRENT MIRROR CIRCUIT

The circuit in which the output current is forced to equal the input current is called as current mirror circuit. In a current mirror circuit, the output current is the mirror image of input current. The current mirror circuit is often referred to a **Current Controlled Current Source or CCCS**.

In figure Q3 & Q4 are perfectly matched,

$$V_{BE3} = V_{BE4}\ and\ I_{B3} = I_{B4}\ \ ,I_{C3} = I_{C4}$$

Applying KCL at Node X

$I_2 = I + I_{C4}$.....(1)

Applying KCL at Node Y

$$I = I_{B3} + I_{B4}\ \ .....(2)$$

Note that

$$I_{B3} = I_{B4}$$
$$I_{C3} = I_{C4}$$

$$I = 2I_{B3} = 2I_{B4}\ .....(3)$$

Substitute equation (3) in equation (1)

$$I_2 = 2I_{B4} + I_{C4} = 2I_{B3} + I_{C3}$$

$$\text{Now}\ \ I_{B3} = \frac{I_{C3}}{\beta}$$

$$I_2 = 2\frac{I_{C3}}{\beta} + I_{C3}$$

$$I_2 = \left[\frac{2}{\beta} + 1\right] I_{C3}$$

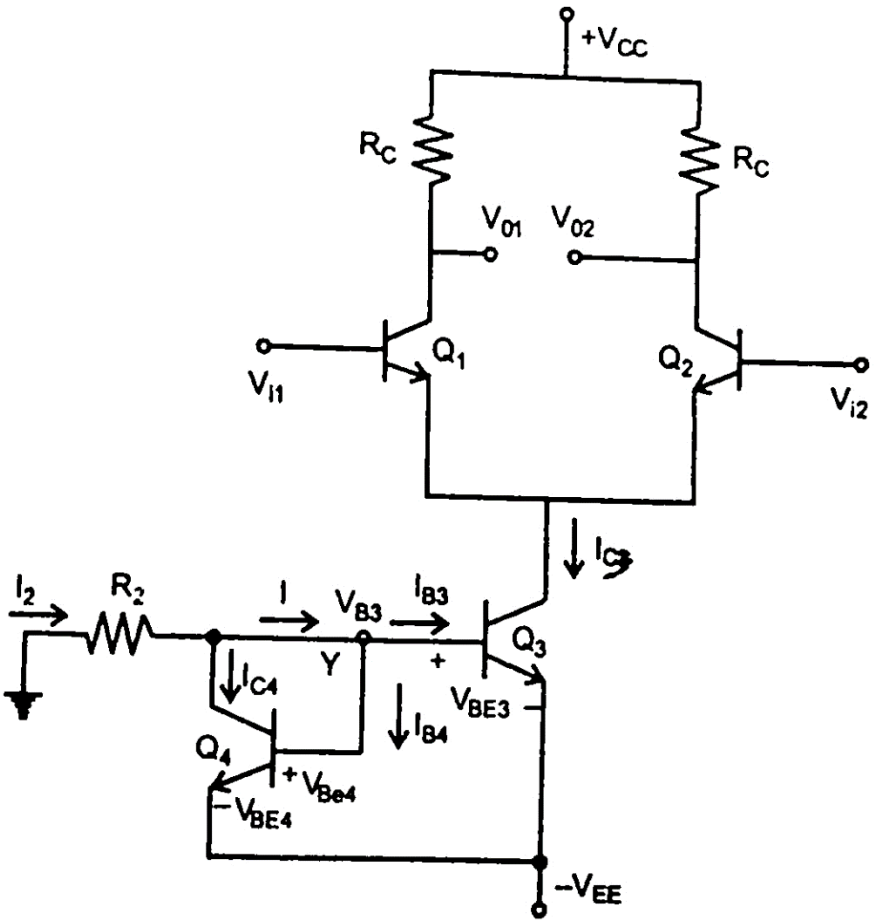


Fig 1.24 : Current Mirror Circuit

Generally β *is very large* $\therefore$ $\frac{2}{\beta}$ *is negligibly small*

$$I_2 \cong I_{C3}$$

Thus Collector current of Q_3 is nearly equal to the current I_2

I_2 can be obtained by applying KVL for the base emitter loop of transistor Q_3

$$-I_2R_2 - V_{BE3} - V_{EE} = 0$$

$$I_2R_2 = V_{EE} - V_{BE3}$$

$$I_2 = \frac{V_{EE} - V_{BE3}}{R_2}$$

By selecting R_2, appropriate I_2 can be set for current mirror circuit

Wilson Current Source Circuit

Another widely used current source using current mirror technique is Wilson current source. High output resistance is the feature of Wilson current source. The Wilson current source circuit is shown in the Fig. 1.25.

The high output resistance is achieved due to the negative feedback through Q3. It also provides base currents cancellation making ***I***, nearly equal to ***I_{ref}***

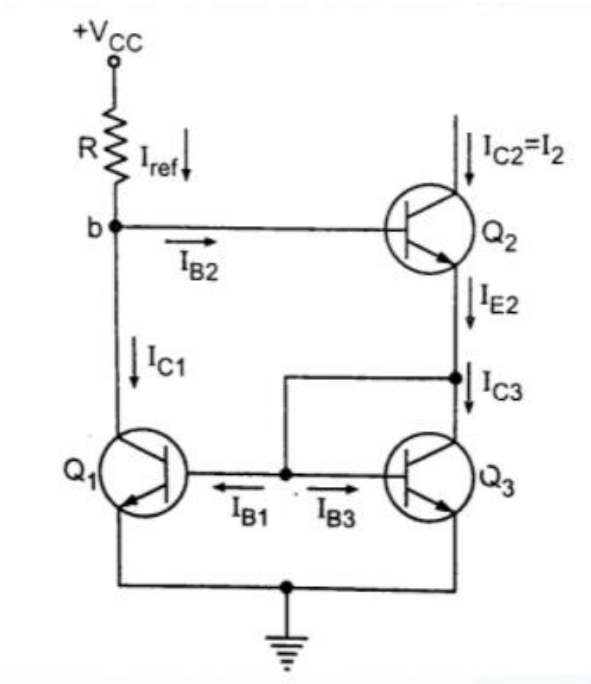


Fig 1.25: ***Wilson Current Source Circuit***

Applying KCL at node b,

$$I_{ref} = I_{C1} + I_{B2} \ldots\ldots (1)$$

$$I_{E2} = I_{C3} + I_{B1} + I_{B3} \ldots\ldots (2)$$

$$\because \; I_{B1} = I_{B2} = I_{B3} = I_B$$

$$I_{E2} = I_{C3} + 2I_B \ldots\ldots (3)$$

$Also\ I_{E2} = I_{C2} + I_{B2}$ also $I_{E2} = I_{C2} + I_B \ldots\ldots\ldots (4)$

$$I_{C2} = I_{E2} - I_B$$

$$I_{C2} = I_{C3} + 2I_B - I_B = I_{C3} + I_B \ldots\ldots\ldots (5)$$

$$I_{C2} = I_{C1}\ as\ all\ transistors\ are\ equal$$

$$\therefore I_{C2} = I_{C1} + I_B \ldots\ldots (6)$$

From equation (1) $I_{ref} = I_{C1} + I_B \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$

Comparing Eqns (6) and (7) We can say

$$I_2 = I_{ref} = I_{C2} \ldots\ldots\ldots\ldots\ldots\ldots (8)$$

Now $I_{E2} = I_{C3} + 2I_B$; $But\ I_B = \frac{I_{C3}}{\beta}$

$$I_{E2} = I_{C3} + 2\frac{I_{C3}}{\beta}$$

$$I_{E2} = I_{C3}\left(1 + \frac{2}{\beta}\right) \quad \ldots\ldots (9)$$

From Equation (4) $I_{E2} = I_{C2} + I_B = I_{C2} + \frac{I_{C2}}{\beta} = I_{C2}\left(1 + \frac{1}{\beta}\right) = \left(\frac{1+\beta}{\beta}\right)$

$$I_{C2} = I_{E2}\left(\frac{\beta}{1+\beta}\right) \ldots\ldots (10)$$

Substitute equation (9) in (10)

$$I_{C2} = I_{C3}\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)$$

$$I_{C3} = \frac{I_{C2}}{\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} \ldots\ldots\ldots (11)$$

From equation (1) $I_{ref} = I_{C1} + I_{B2}$

$$I_{C1} = I_{ref} - I_B$$

$$I_{C1} = I_{ref} - \frac{I_{C2}}{\beta} \ldots\ldots\ldots\ldots (12)$$

Since Transistors are identical $I_{C3} = I_{C1}$

$$\therefore Compairing\ Equations\ (11) and\ (12)$$

$$\frac{I_{C2}}{\left(1 + \frac{2}{\beta}\right)\left(\frac{\beta}{1+\beta}\right)} = I_{ref} - \frac{I_{C2}}{\beta}$$

By solving we get

$$I_{C2}\left(\frac{\beta^2+2\beta+2}{\beta(2+\beta)}\right)=I_{ref}$$

$$I_{C2}=I_{ref}\left(\frac{\beta(2+\beta)}{\beta^2+2\beta+2}\right)=I_{ref}\left(\frac{(\beta^2+2\beta+2-2)}{\beta^2+2\beta+2}\right)$$

$$I_{C2}=I_{ref}\left(1-\frac{2}{\beta^2+2\beta+2}\right)$$

The equation shows that the output current I_{C2} and I_{ref} differ by only a factor which is in the order of $\frac{2}{\beta^2}$.

Widlar Current Source

In operational amplifier low input current is required. Hence input stage is biased at very low current, typically at a collector current of the order of 5 μA. Currents of such low magnitude can be obtained with a modified circuit called Widlar current source. The circuit is shown in the Fig 1.26

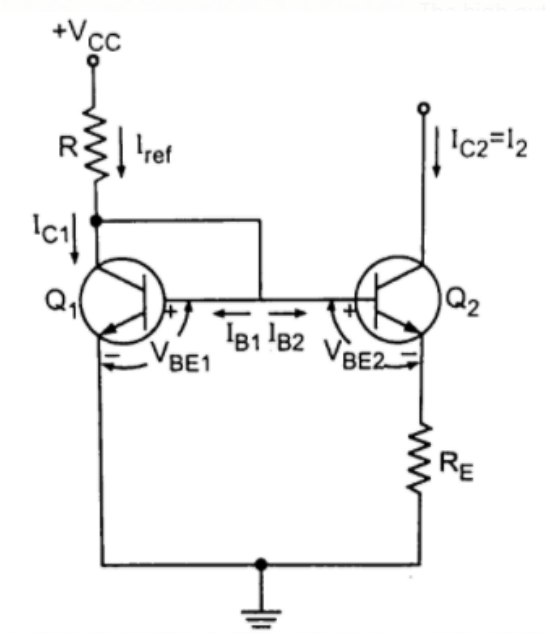


Fig 1.26: Widlar Current Source

The two transistors are identical to each other, but due to emitter resistance R_E, V_{BE1} & V_{BE2} are different. In fact $V_{BE2} < V_{BE1}$ *and hence* $I_{C2} < I_{C1}$ .Due to asymmetric nature of the base emitter loop, the circuits is called "**lens**" rather than a "**mirror**"

Applying KVL in Base emitter loop,

$$V_{BE1}=V_{BE2}+(I_{B2}+I_{C2})R_E \ldots\ldots(1)$$

$$V_{BE1}-V_{BE2}=(I_{B2}+I_{C2})R_E \ldots\ldots(2)$$

For the transistor we can write

$$I_{C1} = I_S \times e^{\frac{V_{BE1}}{V_T}}$$

$$I_{C2} = I_S \times e^{\frac{V_{BE2}}{V_T}}$$

$$\frac{I_{C1}}{I_{C2}} = \frac{I_S \times e^{\frac{V_{BE1}}{V_T}}}{I_S \times e^{\frac{V_{BE2}}{V_T}}} = e^{\left(\frac{V_{BE1}-V_{BE2}}{V_T}\right)}$$

By taking natural log on both sides

$$ln\left(\frac{I_{C1}}{I_{C2}}\right) = \frac{V_{BE1} - V_{BE2}}{V_T}$$

$$V_{BE1} - V_{BE2} = ln\left(\frac{I_{C1}}{I_{C2}}\right) \times V_T \ldots\ldots\ldots (3)$$

Comparing equation (2) and (3)

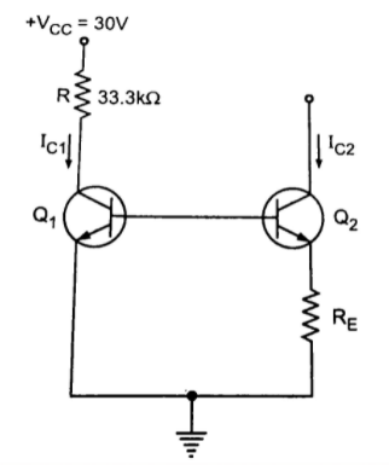
$$(I_{B2} + I_{C2})R_E = ln\left(\frac{I_{C1}}{I_{C2}}\right) \times V_T$$

Neglecting the value of I_{B2} $for\ large\ value\ of\ \beta$,

$$I_{C2} \times R_E = ln\left(\frac{I_{C1}}{I_{C2}}\right) \times V_T \ldots\ldots (4)$$

Problem 1

For the Widlar current source shown in the Fig, design the value of R_E to get I_{C2} as 20 μA. Assume V_{BE} = 0.7 V. Neglect base current.



Solution:

As the Base current is neglected,

$$I_{C1} = \frac{V_{CC} - V_{BE}}{R}$$

$$I_{C1} = \frac{30 - 0.7}{33.3 \times 10^3} = 0.8798\ mA$$

$$I_{C2} = 20\mu A$$

$$I_{C2} \times R_E = V_T \times ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

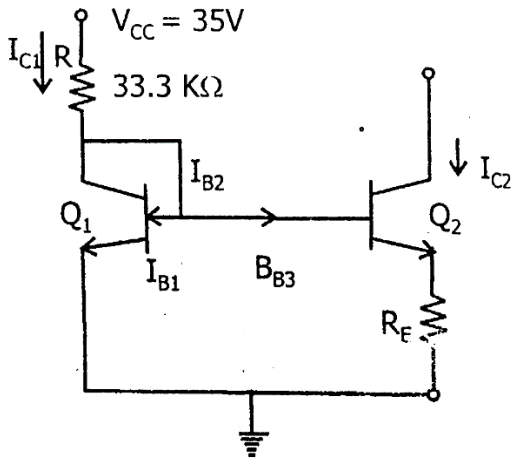
Assuming VT=26mV at room temperature

$$20 \times 10^{-6} \times R_E = 26 \times 10^{-3} \times ln\left(\frac{0.8798\ mA}{20\mu A}\right)$$

$$R_E = 4.92\Omega$$

Problem 2

For the widlar current source shown in Fig design the value R_E to get Ic as 25 mA. Assume V_{BE} = 0.7 V neglect base current.



$$I_{C1} = \frac{V_{CC} - V_{BE}}{R}$$

$$I_{C1} = \frac{35 - 0.7}{33.3K\Omega} = 1.03mA$$

$$I_{C2} = 25mA$$

$$I_{C2} \times R_E = V_T \times ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

Assuming VT=26mV at room temperature

$$25 \times 10^{-3} \times R_E = 26 \times 10^{-3} \times ln\left(\frac{1.03\ mA}{25\mu A}\right)$$

$$R_E = 3.867K\Omega$$